REMARKS

This Amendment addresses the issues outstanding from the final Office Action of December 21, 2007. Applicants respectfully request favorable reconsideration of this application, as amended.

Claims 1-10, 12, 14-17, 21, 24, 25, 27, 28, and 79 are pending, with Claim 1 being the sole independent claim.

Claims 11, 13, 18-20, 22, 23, 26, and 29-78 were previously cancelled without prejudice or disclaimer. By this

Amendment, independent Claim 1 has been amended to recite certain distinctive features of Applicants' invention with greater particularity, as will be discussed below.

In the outstanding Office Action, Claims 1-9, 12, 14, 21, 24, 25, 28, and 79 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hiraki; Claims 10, 15, and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiraki; and Claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hiraki in view of Tanzawa.

Without acceding to the rejections, Claim 1 has been amended more particularly to recite that the dynamic random access memory interface to outside the memory module is arranged to connect to a first memory controller, and the static random access memory interface to outside the memory

module is arranged to connect to a second memory controller, different from the first memory controller.

See, for example, the respective arrangements of the SDRAM IF and the SRAM IF to connect to the SDC and the SRC, respectively, in Applicants' Figure 1.

It is apparent that Hiraki fails to teach or suggest at least the aforementioned features. Hiraki discloses a CPU 10 coupled to each of a flash memory 11, a DRAM 12, and an SRAM 13 via an address bus 15, a data bus 16, a control bus 17, and a RESET line. See Hiraki, Fig. 1. Such an arrangement is evidently quite unlike Applicants' invention, in which a dynamic random access memory interface is arranged to connect to a first memory controller and a static random access memory interface is arranged to connect to a second memory controller, which is different from the first memory controller, as now more particularly claimed.

Tanzawa, which was used as a secondary reference to reject Claims 16 and 17, fails to cure the above-noted deficiencies in Hiraki.

Accordingly, the claims are believed to be allowable over the applied references.

A Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10365) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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